

What is claimed is:

1 1. A memory device with a vertical transistor and a
2 trench capacitor, comprising:

3 a substrate with at least one deep trench;

4 a trench capacitor disposed in the bottom of the deep
5 trench;

6 a conducting wire disposed on the trench capacitor;

7 a trench top insulating layer disposed on the conducting
8 wire, in which the top trench insulating layer
9 consists of a first insulating layer and a second
10 insulating layer surrounded by the first insulating
11 layer; and

12 a control gate disposed on the trench top insulating layer.

1 2. The memory device with a vertical transistor and
2 a trench capacitor of claim 1, further comprising a buried
3 strap in the substrate beside the conducting wire to
4 electrically connect the control gate as a drain.

1 3. The memory device with a vertical transistor and
2 a trench capacitor of claim 1, further comprising a doped area
3 in the substrate beside the control gate as a source.

1 4. The memory device with a vertical transistor and
2 a trench capacitor of claim 1, wherein the first insulating
3 layer is an oxide-nitride layer.

1 5. The memory device with a vertical transistor and
2 a trench capacitor of claim 4, wherein a thickness of the oxide
3 layer is 5 to 10Å.

1 6. The memory device with a vertical transistor and
2 a trench capacitor of claim 4, wherein a thickness of the nitride
3 layer is 40 to 50Å.

1 7. The memory device with a vertical transistor and
2 a trench capacitor of claim 4, wherein the oxide layer is formed
3 by thermal oxidation.

1 8. The memory device with a vertical transistor and
2 a trench capacitor of claim 4, wherein the nitride layer is
3 formed by CVD.

1 9. The memory device with a vertical transistor and
2 a trench capacitor of claim 1, wherein the second insulating
3 layer is BPSG, PSG, NSG or TEOS oxide layer.

1 10. The memory device with a vertical transistor and
2 a trench capacitor of claim 1, wherein a thickness of the second
3 insulating layer is 200 to 400Å.

1 11. The memory device with a vertical transistor and
2 a trench capacitor of claim 1, wherein the second insulating
3 layer is formed by LPCVD.

1 12. The memory device with a vertical transistor and
2 a trench capacitor of claim 1, wherein the conducting wire
3 has a first conducting layer and a second conducting layer ,
4 the conducting wire and the substrate are isolated by a circular
5 insulating layer, and the second conducting layer surrounds
6 the first conducting layer and the circular insulating layer .

1 13. The memory device with a vertical transistor and
2 a trench capacitor of claim 12, wherein the first conducting
3 layer is a doped poly layer or a doped epi-silicon layer.

1 14. The memory device with a vertical transistor and
2 a trench capacitor of claim 12, wherein the second conducting
3 layer is a poly layer or a epi-silicon layer.

1 15. The memory device with a vertical transistor and
2 a trench capacitor of claim 12, wherein the circular insulating
3 layer is a silicon oxide layer.

1 16. The memory device with a vertical transistor and
2 a trench capacitor of claim 1, wherein the control gate consists
3 of a gate conducting layer and a gate oxide layer, and the
4 gate conducting layer consists of a poly layer, a WSi layer,
5 a metal layer, or a composite thereof.

1 17. A method for fabricating a memory device with a
2 vertical transistor and a trench capacitor, comprising:
3 providing a substrate;
4 forming at least one deep trench in the substrate;
5 forming a trench capacitor in the bottom of the deep trench;
6 forming a conducting wire on the trench capacitor;
7 forming a trench top insulating layer on the conducting
8 wire, in which the trench top insulating layer
9 consists of a first insulating layer and a second
10 insulating layer surrounded by the first insulating
11 layer; and
12 forming a control gate on the trench top insulating layer.

1 18. The method for fabricating a memory device with a
2 vertical transistor and a trench capacitor of claim 17, further
3 comprising a buried strap in the substrate beside the conducting
4 wire to electrically connect the control gate as a drain.

1 19. The memory device with a vertical transistor and
2 a trench capacitor of claim 17, further comprising a doped
3 area in the substrate beside the control gate as a source.

1 20. The memory device with a vertical transistor and
2 a trench capacitor of claim 17, wherein the first insulating
3 layer is an oxide-nitride layer.

1 21. The memory device with a vertical transistor and
2 a trench capacitor of claim 20, wherein a thickness of the
3 oxide layer is 5 to 10Å.

1 22. The memory device with a vertical transistor and
2 a trench capacitor of claim 20, wherein a thickness of the
3 nitride layer is 40 to 50Å.

1 23. The memory device with a vertical transistor and
2 a trench capacitor of claim 20, wherein the oxide layer is
3 formed by thermal oxidation.

1 24. The memory device with a vertical transistor and
2 a trench capacitor of claim 20, wherein the nitride layer is
3 formed by CVD.

1 25. The memory device with a vertical transistor and
2 a trench capacitor of claim 17, wherein the second insulating
3 layer is BPSG, PSG, NSG or TEOS oxide layer.

1 26. The memory device with a vertical transistor and
2 a trench capacitor of claim 17, wherein a thickness of the
3 second insulating layer is 200 to 400Å.

1 27. The memory device with a vertical transistor and
2 a trench capacitor of claim 17, wherein the second insulating
3 layer is formed by LPCVD.

1 28. The memory device with a vertical transistor and
2 a trench capacitor of claim 17, wherein the conducting wire
3 has a first conducting layer and a second conducting layer ,
4 the conducting wire and the substrate are isolated by a circular
5 insulating layer, and the second conducting layer surrounds
6 the first conducting layer and the circular insulating layer .

1 29. The memory device with a vertical transistor and
2 a trench capacitor of claim 28, wherein the first conducting
3 layer is a doped poly layer or a doped epi-silicon layer.

1 30. The memory device with a vertical transistor and
2 a trench capacitor of claim 28, wherein the second conducting
3 layer is a poly layer or an epi-silicon layer.

1 31. The memory device with a vertical transistor and
2 a trench capacitor of claim 28, wherein the circular insulating
3 layer is a silicon oxide layer.

1 32. The memory device with a vertical transistor and
2 a trench capacitor of claim 28, wherein the control gate consists
3 of a gate conducting layer and a gate oxide layer, and the
4 gate conducting layer consists of a poly layer, a WSi layer,
5 a metal layer, or a composite thereof.

1 33. A method for fabricating a memory device with a
2 vertical transistor and a trench capacitor, comprising:
3 providing a substrate;
4 forming at least one deep trench in the substrate;
5 forming a trench capacitor in the bottom of the deep trench;
6 forming a insulating layer on the trench capacitor, a
7 sidewall of the deep trench, and the substrate;
8 etching the insulating layer until the insulating layer
9 on the trench capacitor and the substrate is removed
10 to form a circular insulating layer on the sidewall
11 of the deep trench;
12 filling a first conducting layer in the deep trench;
13 etching the first conducting layer to expose the circular
14 insulating layer;
15 etching the circular insulating layer to below the first
16 conducting layer in the deep trench;
17 forming a second conducting layer on the first conducting
18 layer, the circular insulating layer, the sidewall
19 of the deep trench, and the substrate;
20 partially etching the second conducting layer to remove
21 the second conducting layer on the sidewall of the
22 deep trench and the substrate to leave the second
23 conducting layer coning the first conducting layer
24 and the circular insulating layer, in which a
25 conducting wire consists of the first conducting
26 layer and the second conducting layer;
27 conformably forming a first insulating layer on the second
28 conducting layer, the sidewall of the deep trench,
29 and the substrate;

30 partially etching the first insulating layer to remove
31 the first insulating layer on the second conducting
32 layer and the substrate to form a spacer on the
33 sidewall of the deep trench;
34 filling a second insulating layer in the deep trench;
35 etching the second insulating layer to expose the first
36 insulating layer;
37 etching the first insulating layer to remove the first
38 insulating layer on the sidewall above the second
39 insulating layer to leave the second insulating
40 layer on a sidewall of the second insulating layer,
41 in which a trench top insulating layer consists of
42 the first insulating layer and the second insulating
43 layer; and
44 forming a control gate on the trench top insulating layer.

1 34. The method for fabricating a memory device with a
2 vertical transistor and a trench capacitor of claim 33, further
3 comprising a buried strap in the substrate beside the conducting
4 wire to electrically connect the control gate as a drain.

1 35. The memory device with a vertical transistor and
2 a trench capacitor of claim 33, further comprising a doped
3 area in the substrate beside the control gate as a source.

1 36. The memory device with a vertical transistor and
2 a trench capacitor of claim 33, wherein the first insulating
3 layer is an oxide-nitride layer.

1 37. The memory device with a vertical transistor and
2 a trench capacitor of claim 36, wherein a thickness of the
3 oxide layer is 5 to 10Å.

1 38. The memory device with a vertical transistor and
2 a trench capacitor of claim 36, wherein a thickness of the
3 nitride layer is 40 to 50Å.

1 39. The memory device with a vertical transistor and
2 a trench capacitor of claim 36, wherein the oxide layer is
3 formed by thermal oxidation.

1 40. The memory device with a vertical transistor and
2 a trench capacitor of claim 36, wherein the nitride layer is
3 formed by CVD.

1 41. The memory device with a vertical transistor and
2 a trench capacitor of claim 33, wherein the second insulating
3 layer is BPSG, PSG, NSG or TEOS oxide layer.

1 42. The memory device with a vertical transistor and
2 a trench capacitor of claim 33, wherein a thickness of the
3 second insulating layer is 200 to 400Å.

1 43. The memory device with a vertical transistor and
2 a trench capacitor of claim 33, wherein the second insulating
3 layer is formed by LPCVD.

1 44. The memory device with a vertical transistor and
2 a trench capacitor of claim 33, wherein the first conducting
3 layer is a doped poly layer or a doped epi-silicon layer.

1 45. The memory device with a vertical transistor and
2 a trench capacitor of claim 33, wherein the second conducting
3 layer is a poly layer or an epi-silicon layer.

1 46. The memory device with a vertical transistor and
2 a trench capacitor of claim 33, wherein the circular insulating
3 layer is a silicon oxide layer.

1 47. The memory device with a vertical transistor and
2 a trench capacitor of claim 33, wherein the control gate consists
3 of a gate conducting layer and a gate oxide layer, and the
4 gate conducting layer consists of a poly layer, a WSi layer,
5 a metal layer, or a composite thereof.